IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application No.: Patent No.:

Filed: Issue Date:

Title:

Commissioner for Patents
Washington, D.C. 20231

POWER OF ATTORNEY BY ASSIGNEE OF ENTIRE INTEREST
(REVOCATION OF PRIOR POWERS)

As assignee of record of each of the patents listed in the table of attachment A,

REVOCATION OF PRIOR POWERS OF ATTORNEY

all powers of attorney previously given in each of the listed patents are hereby revoked, and

NEW POWER OF ATTORNEY

the following attorneys/agents are hereby appointed to prosecute this patent/application and to transact all business in the Patent and Trademark Office connected therewith: I hereby appoint all attorneys of Thomas, Kayden, Horstemeyer & Risley, LLP, who are listed under the USPTO Customer Number shown below as the attorneys to prosecute this patent/application and to transact all business in the United States Patent and Trademark Office connected therewith, recognizing that the specific attorneys listed under that Customer Number may be changed from time to time at the sole discretion of Thomas, Kayden, Horstemeyer & Risley, LLP, and request that all correspondence about the application be addressed to the address filed under the same USPTO Customer Number:

15650
Patent Trademark Office

Please direct all future correspondence and telephone calls to:

Scott A. Horstemeyer, Reg. No. 34,183
THOMAS, KAYDEN, HORSTEMEYER & RISLEY, L.L.P.
400 Interstate North Parkway
Atlanta, Georgia 30339
770-933-9500

ASSIGNEE OF ENTIRE INTEREST

BROADCOM CORPORATION
5300 California Avenue
Irvine, California 92617-3038

ASSIGNEE CERTIFICATION

The certification under 37 C.F.R. §3.73(b) establishing the right of assignee to take action is attached hereto along with documentation evidencing same. Further, in my official position with Broadcom Corporation, I am authorized to sign documents and otherwise act on its behalf in connection with the management and handling of patent applications and other intellectual property matters.

Date: 9/12/11

Dee Henderson
Director - Intellectual Property Administration
Broadcom Corporation

Attachment A

No.	Patent No	BD No.	Patent Title	Issue Date	BD Assign't (Reel/Frame)
1	7957606	BU5253 050228-4180	SYSTEM AND METHOD FOR EDGE SHARPENING	06/07/11	023811/0361
2	7924944	BU5305 050228-4190	METHOD AND SYSTEM FOR MULTI-BAND DIRECT CONVERSION COMPLIMENTARY METAL-OXIDE-SEMICONDUCTOR (CMOS) MOBILE TELEVISION TUNER	04/12/2011	018067/0536
3	6571181	BU1139 050228-4200	SYSTEM AND METHOD FOR DETECTING A DEVICE REQUIRING POWER	05/27/03	018068/0866
4	7054779	BU1139C1 050228-4210	SYSTEM AND METHOD FOR DETECTING A DEVICE REQUIRING POWER	05/30/06	018068/0866
5	7174259	BU1139C2 050228-4220	SYSTEM AND METHOD FOR DETECTING A DEVICE REQUIRING POWER	02/06/07	018068/0866
6	6954708	BU1139D1 050228-4230	SYSTEM AND METHOD FOR DETECTING A DEVICE REQUIRING POWER	10/11/05	018068/0866
7	7254495	BU1139D1C1 050228-4240	SYSTEM AND METHOD FOR DETECTING A DEVICE REQUIRING POWER	08/07/07	018068/0866
8	6643595	BU1139D2 050228-4250	SYSTEM AND METHOD FOR DETECTING A DEVICE REQUIRING POWER	11/04/03	018068/0866
9	7082372	BU1139D2C1 050228-4260	SYSTEM AND METHOD FOR DETECTING A DEVICE REQUIRING POWER	07/25/06	018068/0866
10	7164659	BU2037 050228-4280	ADAPTIVE GAIN CONTROL BASED ON ECHO CANCELLER PERFORMANCE INFORMATION	01/16/07	012818/0159
11	7177278	BU1434 050228-4290	LATE FRAME RECOVERY METHOD	02/13/07	012818/0848
12	7460479	BU1434C1 050228-4300	LATE FRAME RECOVERY METHOD	12/02/08	012818/0848
13	7254120	BU1436 050228-4310	DATA RATE CONTROLLER	08/07/07	012766/0986
14	7089390	BU1886 050228-4320	APPARATUS AND METHOD TO REDUCE MEMORY FOOTPRINTS IN PROCESSOR ARCHITECTURES	08/08/06	012634/0456
15	7197600	BU2023 050228-4330	TRANSFERRING DATA ALONG WITH CODE FOR PROGRAM OVERLAYS	03/27/07	012614/0097
16	7263074	BU2038 050228-4340	VOICE ACTIVITY DETECTION BASED ON FAR-END AND NEAR-END STATISTICS	08/28/07	012755/0005
17	7835311	BU2038C1 050228-4350	VOICE-ACTIVITY DETECTION BASED ON FAR-END AND NEAR-END STATISTICS	11/16/10	012755/0005
18	7443910	BU1248C1 050228-4360	PHY CONTROL MODULE FOR A MULTI-PAIR GIGABIT TRANSCEIVER	10/28/08	010763/0692

No.	Patent No	BD No.	Patent Title	Issue Date	BD Assign't (Reel/Frame)
19	7151796	BU1805.1 050228-4370	HIGH PERFORMANCE EQUALIZER WITH ENHANCED DFE HAVING REDUCED COMPLEXITY	12/19/06	012600/0177
20	7230982	BU1805C1 050228-4380	DECISION FEEDBACK EQUALIZER FOR MINIMUM AND MAXIMUM PHASE CHANNELS	06/12/07	012613/0855
21	6771196	BU2006.1 050228-4390	PROGRAMMABLE VARIABLE-LENGTH DECODER	08/03/04	013675/0529
22	7580457	BU3336 050228-4400	UNIFIED SYSTEM FOR PROGRESSIVE AND INTERLACED VIDEO TRANSMISSION	08/25/09	015064/0577
23	7995535	BU4737C2 050228-4420	METHOD AND APPARATUS FOR DISTRIBUTING DATA TO A MOBILE DEVICE USING PLURAL ACCESS POINTS	08/09/11	017262/0789
24	7925220	BU6221.13 050228-4430	METHOD AND SYSTEM FOR MATCHING AN INTEGRATED FM SYSTEM TO AN ANTENNA UTILIZING ON-CHIP MEASUREMENT OF REFLECTED SIGNALS	04/12/11	019813/0107
25	7974590	BU6221.2 050228-4440	METHOD AND SYSTEM FOR SIMULTANEOUS SIGNAL TRANSMISSION ON MULTIPLE SELECTED FREQUENCIES	07/05/11	023203/0027
26	7983617	BU6221.5 050228-4450	METHOD AND SYSTEM FOR TRANSMITTING MULTIPLE CHANNELS ON FM BANDS	07/19/11	020544/0637
27	7006563	BU1805 050228-4460	DECISION FEEDBACK EQUALIZER FOR MINIMUM AND MAXIMUM PHASE CHANNELS	02/28/06	012613/0855
28	6304598	BU1021 050228-4470	APPARATUS FOR, AND METHOD OF, REDUCING POWER DISSIPATION IN A COMMUNICATIONS SYSTEM	10/16/01	009422/0821
29	6954490	BU1230C1 050228-4480	FULLY INTEGRATED ETHERNET TRANSMITTER ARCHITECTURE WITH INTERPOLATING FILTERING	10/11/05	010523/0070
30	6459746	BU1247D1 050228-4490	MULTI-PAIR GIGABIT ETHERNET TRANSCEIVER	10/01/02	010694/0029
31	6771725	BU1247D1C1 50228-4500	MULTI-PAIR GIGABIT ETHERNET TRANSCEIVER	08/03/04	010694/0029
32	6411647	BU1230 050228-4510	FULLY INTEGRATED ETHERNET TRANSMITTER ARCHITECTURE WITH INTERPOLATING FILTERING	06/25/02	010523/0070
33	6731691	BU1247C2 050228-4520	MULTI-PAIR GIGABIT ETHERNET TRANSCEIVER HAVING ADAPTIVE DISABLING OF CIRCUIT ELEMENTS	05/04/04	010694/0029
34	7305029	BU1247C2D1 050228-4530	MULTI-PAIR GIGABIT ETHERNET TRANSCEIVER	12/04/07	010694/0029
35	7570701	BU1247C2D1C1 050228-4540	MULTI-PAIR GIGABIT ETHERNET TRANSCEIVER	08/04/09	010694/0029
36	7672368	BU1248D1	PHY CONTROL MODULE FOR A MULTI-PAIR GIGABIT TRANSCEIVER	03/02/10	010228/0504

No.	Patent No	BD No.	Patent Title	Issue Date	BD Assign't (Reel/Frame)
		050228-4550			
37	7933341	BU1338.1 050228-4560	SYSTEM AND METHOD FOR HIGH SPEED COMMUNICATIONS USING DIGITAL SIGNAL PROCESSING	04/26/11	011921/0320
38	6477200	BU1247 050228-4570	MULTI-PAIR GIGABIT ETHERNET TRANSCEIVER	11/05/02	010694/0029
39	6898238	BU1201C1 050228-4580	APPARATUS FOR, AND METHOD OF, REDUCING POWER DISSIPATION IN A COMMUNICATIONS SYSTEM	05/24/05	009422/0821
40	7194028	BU1247C2D2 050228-4590	MULTI-PAIR GIGABIT ETHERNET TRANSCEIVER HAVING DECISION FEEDBACK EQUALIZER	03/20/07	010694/0029
41	7453935	BU1247C2D2C1 50228-4600	MULTI-PAIR GIGABIT ETHERNET TRANSCEIVER HAVING DECISION FEEDBACK EQUALIZER	11/18/08	010694/0029
42	7197069	BU1247C2D3 050228-4610	MULTI-PAIR GIGABIT ETHERNET TRANSCEIVER HAVING ADAPTIVE DISABLING OF CIRCUIT ELEMENTS	03/27/07	010694/0029
43	7792186	BU1247C2D3C1 050228-4620	MULTI-PAIR GIGABIT ETHERNET TRANSCEIVER HAVING A SINGLE-STATE DECISION FEEDBACK EQUALIZER	09/07/10	010694/0029
44	7194029	BU1247C2D4 050228-4630	Multi-pair gigabit ethernet transceiver having adaptive disabling or circuit elements	03/20/07	010694/0029
45	6928106	BU1248 050228-4640	PHY CONTROL MODULE FOR A MULTI-PAIR GIGABIT TRANSCEIVER	08/09/05	010763/0692
46	7801240	BU1247C2D2C2 050228-4650	MULTI-PAIR GIGABIT ETHERNET TRANSCEIVER	09/21/10	010694/0029
47	7801241	BU1247C2D2C3 050228-4660	MULTI-PAIR GIGABIT ETHERNET TRANSCEIVER	09/21/10	010694/0029
48	6823483	BU1248.1 050228-4670	PHYSICAL CODING SUBLAYER FOR A MULTI-PAIR GIGABIT TRANSCEIVER	11/23/04	010764/0358
49	7983569	BU1338 050228-4680	HIGH-SPEED TRANSMISSION SYSTEM FOR OPTICAL CHANNELS	07/19/11	011679/0588
50	7379498	BU2094 050228-4690	RECONSTRUCTING A COMPRESSED STILL IMAGE BY TRANSFORMATION TO A COMPRESSED MOVING PICTURE IMAGE	05/27/08	012693/0858
51	6411117	BU1249 050228-4700	DYNAMIC REGISTER WITH IDDQ TESTING CAPABILITY	06/25/02	010393/0131
52	6965610	BU1272 050228-4710	SYSTEM AND METHOD FOR PROVIDING COMPATIBILITY BETWEEN DIFFERENT TRANSCEIVERS IN A MULTI-PAIR COMMUNICATION SYSTEM	11/15/05	012458/0191
53	7668108	BU1426C1 050228-4720	PERFORMANCE INDICATOR FOR A HIGH-SPEED COMMUNICATION SYSTEM	02/23/10	011948/0396
54	7965647	BU1426C2	PERFORMANCE INDICATOR FOR A HIGH-	06/21/11	011948/0396

No.	Patent No	BD No.	Patent Title	Issue Date	BD Assign't (Reel/Frame)
		050228-4730	SPEED COMMUNICATION SYSTEM		
55	6449110	BU4745 050228-4740	OPTIMIZING OPERATION OF A DISK STORAGE SYSTEM BY INCREASING THE GAIN OF A NON-LINEAR TRANSDUCER AND CORRECTING THE NON-LINEAR DISTORTIONS USING A NON-LINEAR CORRECTION CIRCUIT	09/10/02	014428/0418
56	6032284	BU4752 050228-4750	TRELLIS CODING SYSTEM FOR DISC STORAGE SYSTEMS	02/29/00	014428/0418
57	6505320	BU4763 050228-4760	MULTIPLE-RATE CHANNEL ENDEC IN A COMMUTED READ/WRITE CHANNEL FOR DISK STORAGE SYSTEMS	01/07/03	014428/0418
58	6865234	BU1082 050228-4770	PAIR-SWAP INDEPENDENT TRELLIS DECODER FOR A MULTI-PAIR GIGABIT TRANSCEIVER	03/08/05	010522/0499
59	6185261	BU1201 050228-4780	DETERMINATION OF TRANSMITTER DISTORTION	02/06/01	010373/0004
60	6731914	BU1201C1 050228-4790	DETERMINATION OF TRANSMITTER DISTORTION	05/04/04	010373/0004
61	7068982	BU1201C1 050228-4800	DETERMINATION OF TRANSMITTER DISTORTION	06/27/06	010373/0004
62	7369608	BU1231C2 050228-2810	DYNAMIC REGULATION OF POWER CONSUMPTION OF A HIGH-SPEED COMMUNICATION SYSTEM	05/06/08	010228/0504
63	6762762	BU1267C1 050228-4820	GRAPHICS ACCELERATOR	07/13/04	011368/0527
64	6201831	BU1287 050228-4830	DEMODULATOR FOR A MULTI-PAIR GIGABIT TRANSCEIVER	03/13/01	010605/0173
65	7656938	BU1287C2 050228-4840	DEMODULATOR FOR A MULTI-PAIR GIGABIT TRANSCEIVER	02/02/10	010605/0173
66	7936840	BU1287C3 050227-4850	DEMODULATOR FOR A MULTI-PAIR GIGABIT TRANSCEIVER	05/03/11	010605/0173
67	7970124	BU2037C1 050228-4860	ADAPTIVE GAIN CONTROL BASED ON ECHO CANCELLER PERFORMANCE INFORMATION	06/28/11	012818/0159
68	6861834	BU1404 050228-4870	SYSTEM AND METHOD FOR MEASURING THE POWER CONSUMED BY A CIRCUIT ON A PRINTED CIRCUIT BOARD	03/01/05	011942/0526
69	7034897	BU2019 050228-4270	METHOD OF OPERATING A VIDEO DECODING SYSTEM	04/25/06	012761/0060
70	7680455	BU3533.1 050228-4410	METHOD AND SYSTEM FOR ANTENNA SELECTION DIVERSITY WITH BIASING	03/16/10	023759/0484